



04/25/97

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application  
 Commissioner of Patents and Trademarks  
 Washington, D.C. 20231

59383 U.S. PTO

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04/25/97

## NEW APPLICATION TRANSMITTAL

Please find enclosed herewith for filing, the patent application of

Inventor(s): **Ritu Shrivastava and Chitranjan N. Reddy**  
 For (title): **FLASH EPROM ARRAY WITH SELF-ALIGNED SOURCE CONTACTS AND PROGRAMMABLE SECTOR ERASE ARCHITECTURE**

## 1. Type of Application

This transmittal is regarding an:

- |                                     |          |                          |                            |
|-------------------------------------|----------|--------------------------|----------------------------|
| <input checked="" type="checkbox"/> | Original | <input type="checkbox"/> | Divisional                 |
| <input type="checkbox"/>            | Design   | <input type="checkbox"/> | Continuation               |
| <input type="checkbox"/>            | Plant    | <input type="checkbox"/> | Continuation-in-Part (CIP) |

## 2. Benefit of Prior U.S. Application(s) (35 U.S.C. §120)

- ☒ The new application being transmitted does not claim the benefit of any prior application(s).
- ☐ The new application being transmitted claims the benefit of prior U.S. application(s) and enclosed are "ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED."

## 3. Papers Required for Filing Date

Applicant(s) submits herewith the following papers pursuant to 37 C.F.R. §1.53(b)

- 16 Pages of Specification  
 7 Pages of Claims  
 1 Pages of Abstract  
 19 Pages of Drawings

- ☒ Formal drawings  
☐ Informal drawings

- ☐ Applicant has enclosed photographs as drawings. Pursuant to 37 C.F.R. §1.84(b), included is a PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)

## CERTIFICATE OF MAILING (C.F.R. 1.10)

I hereby certify that this New Application Transmittal and documents referred to as enclosed therein are being deposited with the United States Postal Service on this date April 25, 1997 in an envelope as "Express Mail Post Office to Addressee"  
 Mailing Label Number EH 7138 32 766 US addressed to the Commissioner of Patents and Trademarks,  
 Washington, D.C. 20231

Name of person mailing paper:

*Paula Chin*

Signature of person mailing paper:

*[Signature]*

**4. Additional papers enclosed**

- ☐ Preliminary Amendment
- ☒ Information Disclosure Statement
- ☒ Form PTO-1449
- ☐ Citations
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☐ Other

**5. Declaration or Oath**

Pursuant to 37 C.F.R. §1.63 Applicant submits herewith

- ☒ A declaration executed by
  - ☒ inventor(s)
  - ☐ legal representatives of inventor(s)
  - ☐ joint inventor or person showing proprietary interest on behalf of inventor who refused to sign or cannot be reached.Pursuant to 37 C.F.R. §1.47 Applicant includes herewith the required petition and statement.
- ☐ A Declaration or Oath is NOT included
  - ☐ Application is made by a person authorized under 37 C.F.R. §1.41(c) on behalf of all the above named inventor(s).
  - ☐ A showing is also made showing that the filing is authorized.

**6. Language of Application**

The language of the application is:

- ☒ English, pursuant to 37 C.F.R. §1.52(a)
- ☐ Not English
  - ☐ the attached translation is a verified translation pursuant to 37 C.F.R. §1.52(a).
  - ☐ included is the fee set forth under 37 C.F.R. §1.17(k)
  - ☐ a verified translation pursuant to 37 C.F.R. §1.2(a) and the required fee set forth under 37 C.F.R. §1.17(k) will be submitted within the time set by the Patent Office.

**7. Assignment and Recordal of Assignment**

- ☒ Applicant(s) has assigned the invention to:

**ALLIANCE SEMICONDUCTOR CORPORATION**

- ☒ The assignment is submitted herewith for recordal. Pursuant to 37 C.F.R. §3.28 a separate assignment cover sheet is also attached.
- ☐ The assignment for recordal will follow.

**8. Claim of Foreign Priority**

- ☒ Applicant(s) do(es) NOT claim priority from a prior foreign application.
- ☐ Applicant(s) claim(s) foreign priority pursuant to 35 U.S.C. §119 and §172. In accordance with 37 C.F.R. §1.55 the foreign applications are identified below:

<u>Country</u>	<u>Application Number</u>	<u>Filing Date</u>
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certified copies of these applications

☐ is (are) attached.

☐ will follow.

**9. Filing Fee Calculation**

- A. ☒ Original Application

Basic fee:				=	\$ 770.00
Fee for Claims in Excess of Twenty:	29	- 20 =	9	x 22 =	\$ 198.00
Fee for Ind. Claims in Excess of Three:	3	- 3 =	0	x 80 =	\$ 0.00
Fee for Multiple Dependent Claim(s):	0			+260 =	\$ 0.00
Total filing fee:					<b>\$968.00</b>

- ☐ An amendment canceling extra claims enclosed.
- ☐ An amendment deleting multiple-dependencies enclosed.
- ☐ The fee for extra claims is not being paid at this time.

- B. ☐ Design Application

Basic Fee----- \$320.00

Total Filing Fee Calculation \$ n/a

- C. ☐ Plant Application

Basic Fee----- \$530.00

Total Filing Fee Calculation \$ n/a

**10. Small Entity Statement(s) and Reduction of Fees Therefor**

- ☐ A Verified Statement(s) Claiming Small Entity Status for this application is attached, pursuant to 37 C.F.R. §1.27 is attached.

Total from part 10A, 10B or 10C, above: \$ 0.00  
(reduced by half)

Filing Fee Calculation \$ n/a

**11. Request for International -Type Search Per 37 C.F.R. §1.104(d)**

- ☐ Please prepare an international-type search report for this application at the time when the national examination on the merits takes place.

**12. Total Fee Payment For This Transmittal**

- ☐ No fees are enclosed at this time  
☐ No filing fee is being paid at this time.

☒ Fees paid at this time

<input checked="" type="checkbox"/>	Filing fee	\$ 968.00
<input checked="" type="checkbox"/>	Assignment recordal fee	\$ 40.00
<input type="checkbox"/>	Petition fee for filing by other than all of the inventors or person on behalf of the inventor who refused to sign or cannot be reached (\$130.00)	\$ .00
<input type="checkbox"/>	Processing fee for an application with a specification in a non-English language (\$130.00)	\$ .00
<input type="checkbox"/>	Processing and retention fee (\$130.00)	\$ .00
<input type="checkbox"/>	international-type search report fee (\$40.00)	\$ .00
Total fees:		<b>\$1008.00</b>

**13. Method of Payment of Fees**

- ☐ Check in the amount of \$ \_\_\_\_\_  
☒ Charge account no. 01-0886 in the amount of \$ 1,008.00.  
A duplicate of this transmittal is attached.

**14. Authorization to Charge Additional Fees**

- ☒ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 01-0886.
- ☒ 37 C.F.R. §1.16(a), (f) or (g) (filing fees)  
☒ 37 C.F.R. §1.16(b), (c) and (d) (presentation of extra claims)  
☐ 37 C.F.R. §1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)  
☒ 37 C.F.R. §1.17 (application processing fees)  
☐ 37 C.F.R. §1.18 (issue fee at or before mailing Notice of Allowance, pursuant to 37 C.F.R. §1.311(b))

**15. Instructions as to Overpayment**

- ☒ Please Credit Account No. 01-0886.  
☐ Refund

**16. Signature by Attorney or Agent**

Respectfully submitted,

APRIL 25, 1997  
Date

Bradley T. Sako  
Bradley T. Sako

Reg. No.: 37,923  
Telephone: (408) 383-4900  
Facsimile: (408) 383-4999

ALLIANCE SEMICONDUCTOR  
CORPORATION  
3099 North First Street  
San Jose, California 95134-2006

**[X] Incorporation by reference of added pages**

[ ] Plus Added Pages For New Application Transmittal Where Benefit Of  
Prior U.S. Application(s) Claimed

Number of added pages \_\_\_\_.

[X] Plus Added Pages For Papers Referred To In Item 4 Above

Number of added pages 152

**[ ] Statement Where No Further Pages Added**

[ ] This transmittal ends with this page.

# FLASH EPROM ARRAY WITH SELF-ALIGNED SOURCE CONTACTS AND PROGRAMMABLE SECTOR ERASE ARCHITECTURE

## TECHNICAL FIELD

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The present invention relates generally to nonvolatile memory integrated circuits and more particularly to flash EPROM arrays.

## BACKGROUND OF THE INVENTION

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Nonvolatile memory integrated circuits typically include memory cells arranged in one or more arrays. A common type of nonvolatile memory integrated circuit is an electrically programmable read-only-memory (EPROM). The memory cells of EPROMs commonly utilize floating gate structures which can store charge, and thereby indicate a certain logic state. Electrically programmable ROMs include UVPROMs in which wherein the cells are programmed by hot electron injection or tunneling, and erased by the application of ultra-violet light; EEPROMs in which the cells are programmed and erased by tunneling; and "flash" EPROMs in which the cells are programmed by hot electron injection or tunneling, and groups of cells are simultaneously erased by tunneling.

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The reading, programming, and erasing of EPROM memory cells requires the application of certain voltages to each cell. For example, in U.S. Patent No. 4,698,787 issued to *Mukherjee et al.* on October 6, 1987, a flash EPROM is disclosed having one transistor ("1-T") cells where the cells are read by grounding the sources of the cells, applying a positive voltage to the gate, and sensing the resulting potential at the drain. The cells of *Mukherjee et al.* are programmed by grounding the sources of the cells, and applying a positive gate and drain voltage. Erasure of the cells of *Mukherjee et al.* is accomplished by floating the drains of a group of cells, and placing the sources of the cells in the group at a higher potential than their respective gates. In *Mukherjee et al.*, because the memory cells are flash erased there is no need to differentiate source connections. As a result, a common source diffusion is utilized. The use of a common source diffusion leads to a compact array design.

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The use of a common source diffusion can give rise to a number of limitations in the implementation of a flash EPROM. For example, when a selected cell coupled to the common source diffusion is programmed, the inherent resistance of

the diffused region can result in the poor programming of selected cells, due to the source potential generated by the programming current. Accordingly, the size of common source regions in flash EPROMs are limited to minimize common source resistance. In addition, in the case where the erase voltage between the control gate and the source is accomplished by placing the sources at a higher potential with respect to the gate and also with respect to the substrate, substrate junction leakage can result. Such junction leakage can result in source current which can affect erase speed due to source voltage drop. Alternately, a process requiring a higher source breakdown voltage may be needed. For example, *Mukherjee et al.* employs a double diffused source region to increase the source breakdown voltage. U.S. Patent No. 4,742,492 issued to *Smayling et al.* on May, 3 1988, and U.S. Patent No. 5,077,691 issued *Haddad et al.* on December 31, 1991 disclose the use of a negative word line erase potential in conjunction with a relatively low positive common source voltage to limit the substrate-to-source potential during erase.

Yet another issue raised by diffused common source regions is the array area required for such approaches. Referring now to Fig. 1a, a portion of a prior art flash EPROM array is set forth in a top plan view. The portion of the array set forth includes a three rows of cells, shown as items 1a-1c. Each row of cells includes memory cells 2a-2c and 3a-3c. Each memory cell includes a floating gate (indicated by diagonal hatching), a control gate formed over the floating gates of each row (indicated by horizontal hatching), and source and drain regions separated by channel regions. The drain regions are designated as 4a-4c and 5a-5c. Bit line contacts 6a-6d are provide for coupling the drain regions of the memory cells to bit lines (not shown). Each bit line contact 6a-6d is shared by two memory cells from different rows. Memory cells 2a, 2b, 3a and 3b share a common source region 7 that extends in the row direction. In the arrangement of Fig. 1a, the common source region 7 is formed as part of an active region separated by isolation regions. The active regions are created prior to the formation of the control gate of the memory cells 2a-2c and 3a-3c. As a result, in order to ensure that misalignments inherent in the fabrication process will not create memory cells having control gates overlap the source region, the control gates must be formed at a minimum distance away from source region. The minimal spacing requirement results in larger arrays.

In the previous art, all the source contacts are tied together because of the need to minimize source resistance. Erase voltages are typically supplied to the common sources by a "strapping" interconnect, such as metal. This type of arrangement

does not allow smaller portions of the array to be erased at will, and results in arrays having minimum, predetermined erasable portions ("granularity").

Fig. 1b sets forth a prior art approach to eliminating the source spacing requirement by fabricating a "self-aligned" common source region. Fig. 1b has many of the same features of Fig. 1a, and so like elements will be referred to by the same reference character. The self-aligned common source of Fig. 1b differs from the arrangement of Fig. 1a in that the source regions includes active area source regions 7a and etched source regions 7b. As in the case of the Fig. 1a, the active area source regions 7a are formed prior to the control gates of the memory array. Unlike Fig. 1a, the etched source regions 7b are created after the floating gate and control gate are formed, by etching through field oxide regions and implanting dopants into the exposed etched source region to increase the conductivity of the source. While allowing memory cells to be placed closer to the source region, the self-aligned common source region approach, such as that set forth in Fig. 1b includes some drawbacks. Despite the implantation step, the resulting resistance of the common source introduces a limit to the number of memory cells that may be coupled to the common source before periodic contacts using a low resistance interconnect such as metal must be made to the source region. A periodic contact 8 for the common source region is set forth Fig. 1b. As shown in the figure, the periodic contact requires its own active area and so disturbs the pitch of the memory cells, reducing the compactness of the resulting array. Another issue raised by the self-aligned common source region such as that set forth in Fig. 1b, is illustrated by Fig. 1c. Fig. 1c is a side cross sectional view taken along line c-c in Fig. 1b. Fig. 1c sets forth portions of memory cells 3a and 3b, which both include control gates (word lines) 9a and 9b, and floating gates 10a and 10b. The control gates and floating gates are protected on their side surfaces by a source sidewall spacers 11, and drain sidewall spacers 12. The memory cells (3a and 3b) along line c-c sit on a insulation area formed from field oxide 13. In order to form the etched source region 7b, a trench 14 must be etched through the field oxide 13 in a self-aligned source etch step. The action of etching through the field oxide 13 results in some etching of the source sidewall spacers 11, which can lead to charge leakage in the memory cell, impacting the reliability of the memory device.

It would be desirable to arrive at an EPROM array without the drawbacks of prior art approaches.



## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a non-volatile memory cell array having a reduced area by eliminating the need of source "strapping".

5 It is another object of the present invention to provide a non-volatile memory cell array having flexible, user programmable common source blocks or sectors.

It is another object of the present invention to provide a flash EPROM device wherein parts of the array can be selectively erased by choosing source interconnect lines.

10 It is another object of the present invention to provide an improved "page erase" architecture.

It is another object of the present invention to provide a user programmable sector erase architecture.

15 It is another object of the present invention to provide a non-volatile memory cell array having a low resistance common source arrangement.

It is another object of the present invention to increase the number of non-volatile memory cells that can have common source connections in an array.

It is another object of the present invention to improve the uniformity of programming and erase speeds in a flash EPROM.

20 It is another object of the present invention to improve cell endurance of flash EPROM devices.

It is another object of the present invention to provide a flash EPROM having improved low supply voltage operation.

25 It is another object of the present invention to reduce cell current programming and erase variations.

It is another object of the present invention to reduce the number of source contacts required in non-volatile memory array.

It is another object of the present invention to improve the reliability of flash EPROMs by eliminating the need for a self-aligned source etch step.

30 The present invention includes a non-volatile memory cell array where each memory cell has a source region. An inter-layer dielectric is formed over the memory cells and the source regions. A self-aligned contact etch is applied to expose the source regions. The source regions are then commonly connected by a conductive layer formed over the exposed source regions.

According to one aspect of the present invention, the memory cells are formed from polycrystalline silicon (polysilicon) layers, and the conductive layer connecting the source regions is formed from polysilicon.

According to another aspect of the present invention, the source region of one memory cells in one row is shared by the source region of another memory cell in an adjacent row.

According to another aspect of the invention, the etch mask used to expose the source regions has an opening that extends along the row of the array.

According to another aspect of the invention, the etch mask used to expose the source regions has an opening corresponding to each source region that is to be exposed.

An advantage of the present invention is that it improves programming in a flash EPROM by reducing voltage drop on the source lines.

Another advantage of the present invention is that it provides a more scalable technology by using a polysilicon layer to interconnect source regions, rather than a metal contacts. Metal contacts can give rise to processing problems due to the high aspect ratios of such metal contact.

Another advantage of the present invention is that it provides a flash EPROM having a more flexible architecture.

Other objects and advantages of the present invention will become apparent in light of the following description thereof.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a-1c illustrate flash EPROM arrays according to the prior art.

Figs. 2a-2c set forth a flash EPROM array according to a preferred embodiment of the present invention.

Figs. 3a-3c through Figs. 9a-9c illustrate a process for fabricating a flash EPROM array according to the present invention.

Fig. 10 is a flow diagram illustrating a method of fabricating a flash EPROM array according to the present invention.

Fig. 11 is a block schematic diagram illustrating a source decoding scheme according to the present invention.

## DETAILED DESCRIPTION OF THE EMBODIMENTS

The preferred embodiment of the present invention is flash EPROM array having a plurality of one transistor (1-T) stacked gate non-volatile memory cells arranged in rows and columns. A portion of an array according to the preferred embodiment is set forth generally, in Figs. 2a-2c. Fig. 2a is a top plan view. Fig. 2b is a side cross sectional view taken along line b--b of Fig. 2a (the row direction). Fig. 2c is a side cross sectional view taken along line c--c of Fig. 2a (the column direction). The array is designated by the general reference character **100** and is formed on a semiconductor substrate **102**. The portion of the array **100** set forth includes four rows designated as **104a-104d**, and three columns, shown as **106l-106n**. The portion of the array **100** set forth in Fig. 2a includes twelve memory cells (**108a,l-108d,n**) identified according to their column and row location.

Each of the memory cells (**108a,l-108d,n**) includes a floating gate **110** (indicated by vertical hatching) and a control gate. The control gates of the memory cells in the same row (**104a-104d**) are formed as integral portions of a wordline **112** (indicated by horizontal hatching) that extends along each row (**104a-104d**). Each memory cell (**108a,l-108d,n**) also includes a drain region (**114b,l-114d,n**) and a source region. In the preferred embodiment the drain regions (**114b,l-114d,n**) of the memory cells in different rows are coupled to bit line contacts **116a-116f**. For example, in Fig. 2a, drains **114b,l** and **114c,l** are coupled to the bit line contact **116a**.

The memory cell source arrangement of the preferred embodiment, includes source regions **118a-118f** that are shared between cells in adjacent rows. For example, in Fig. 2a, source region **118a** is shared between memory cells **108a,l** and **108b,l**. Unlike the prior art, the source regions of memory cells in adjacent columns remain isolated, on the substrate level, by isolation regions. As set forth in Fig. 2a, source region **118b** is separated from source regions **118a** and **118c** by isolation regions **120**. Although isolated from one another on the substrate level, the source regions **118a-118f** are commonly connected by low resistance source conductor members **122a-122b** (indicated by diagonal hatching) formed after the memory cells (**108a,l-108d,n**). The source conductor members **122a-122b** of the preferred embodiment, extend along row pairs, partially overlapping the memory cells of the their respective rows. As set forth in Fig. 2a, source conductor

member **122a** extends along rows **104a** and **104b**, while source conductor member **122b** extends along rows **104c** and **104d**.

It is noted that the bit lines are excluded from the view of Fig. 2a for clarity. In the preferred embodiments a bit line is associated with each column, and extends in the column direction, perpendicular to the wordlines, over the memory cells and source conductor members. Each bit line makes contact with the drains of the memory cells of its associated column.

Referring now to Fig. 2b, a side cross sectional view of source region **118b** taken along the row direction, is set forth in detail. The source region **118b** is shown formed in an active area **124** of the substrate **102**, and isolated on both sides by isolation regions **120**. Along the direction of the Fig. 2b, the source conductor member **122a** is shown to be formed on the isolation regions **120** and extend down to the active area **124** to make contact with the source region **118b**. In the preferred embodiment, the source conductor members are formed from a third layer of polycrystalline silicon (poly 3) **126** and a layer of silicide **128**. An inter-layer dielectric (ILD 2) **130** is formed over the source conductor member **118b**. Unlike Fig. 2a, a bit line **132** is shown in Fig. 2b, formed on the ILD 2 **130**, running in the column direction.

Referring now to Fig. 2c, a side cross sectional view is set forth, taken along the line c-c of Fig. 2a, through memory cells **108a,m** and **108b,m**. The memory cells **108a,m** and **108b,m** are shown formed on an active area **124** of the substrate **102**, sharing source region **118b**. Each memory cell includes a wordline (control gate) **112** and a floating gate **110**. The floating gate is formed from polysilicon (poly 1) and the wordlines, like the source conductor members, are formed from a layer of polysilicon (poly 2) **134** and a layer of silicide **136**. The floating gates **110** are insulated from the active area **124** by tunnel dielectric **138**, and from their respective wordlines **112** by a cell interlayer (interpoly) dielectric **140**. The sides of the floating gate/control gate pairs are insulated by drain sidewall spacers **142** and source sidewall spacers **144**. The top of the control gates **112** are insulated by a "cap" insulator **146**.

Referring once again to Fig. 2c, in the preferred embodiment, the source conductor member **122a** is disposed over both memory cells (**108a,m** and **108b,m**), and extends downward, along the source sidewall spacers **144** to make contact with source region **118b**. The source sidewall spacers **144** and cap insulators **146** are formed from an insulating material, and insulate the wordlines **112** and control gates **110** of the memory cells (**108a,m** and **108b,m**). It is noted that unlike the

self-aligned common source arrangement of Figs. 1b and 1c which etches through the field oxide regions to expose the substrate in forming a common source, the preferred embodiment only clears each source region (118a-118f) in the active areas, resulting in far less thinning of the source sidewall spacers 144 and interlayer dielectric 140, for more reliable memory cells. A portion of the source conductor member 122a is disposed on a first inter-layer dielectric (ILD 1) 148. The ILD 2 130 is shown formed over the source conductor member 122a and the ILD 1 148. As in the case of Fig. 2b, the bit line 132 is formed on the ILD 2 130. In the preferred embodiment, the bit line 132 includes a plug member 149 that provides reliable electrical contact to the drain region 116b.

Referring now to Figs. 3a-3c through Figs. 9a-9c in conjunction with Fig. 10, a series of plan views, side cross sectional views, and a flow chart are set forth, illustrating the fabrication of a flash EPROM array according to a preferred embodiment of the present invention.

The plan view and side cross sectional views correspond to those set forth in Figs. 2a-2c. Those figures having numbers followed by the letter "a" (e.g., Figs. 3a, 4a, 5a...) are the same top plan view taken at various stages in the process set forth in Fig. 10. In the same manner, those figures having numbers followed by the letters "b" and "c" (e.g., Figs. 3b, 4b, 5b... Figs. 3c, 4c, 5c...) are side cross sectional views taken along the same lines b-b and c-c at various stages in the process.

Referring now to Fig. 10 in conjunction with Figs. 3a-3c, the process 200 begins with an isolation process such as a LOCOS step 202. Isolation regions 120 of field oxide are formed in the substrate 102 separated by active areas 124. Notably, unlike the diffused source case in Fig. 1a, there is no active area running horizontally, connecting vertically disposed active areas.

Following the isolation 202 and channel implant 204 steps, the sacrificial oxide (which is disposed over the active areas 124) is etched away (step 206) to create a cleaned active area 124. In the preferred embodiment, the sacrificial oxide etch is a wet chemical etch of dilute hydrofluoric acid (HF). In step 206, and as shown in Figs. 3a-3c, the tunnel dielectric 138 is grown on the active area 124. In the preferred embodiment, the tunnel oxide is thermally grown for a thickness in the approximate range of 80-100 Å.

Referring now to Figs. 4a-4c, following the growth of the tunnel dielectric 128, a first layer of polysilicon (poly 1) is deposited (step 210). The poly 1 layer conformally covers tunnel dielectric 138 and the isolation regions 120. In the

preferred embodiment, the poly 1 layer is deposited using a conventional polysilicon deposition process resulting in amorphous or polycrystalline grain structures. Doping of the poly 1 can be done in situ, or by using ion implantation. Typical deposition temperatures are  $\sim 570^{\circ}\text{C}$  for amorphous silicon, and  $\sim 630^{\circ}\text{C}$  for polycrystalline silicon. An in situ doping technique using phosphoryl trichloride ( $\text{POCl}_3$ ), or ion implant may be used to dope the poly 1 layer. For ion implantation, typical phosphorous implant doses are approximately  $5 \times 10^{15}/\text{cm}^2$  at an energy of 30 KeV. The resulting preferred vertical thickness of the poly 1 layer is approximately 500-1500 Å. Step 212 of Fig. 10, involves patterning a first floating gate structure, referred to in this description as a floating gate "slab." In the preferred embodiment this step includes the etching of the poly 1 layer. A poly 1 etch mask of photoresist is developed along the channel length of the EPROM cell to pattern the floating gate as in a conventional 1-T cell flash EPROM process. The poly 1 is subjected to an etch which etches through the poly 1 down to the field oxide 120 creating floating gate "slab" 150 structures that cover the memory cell channel regions. Three such floating gate slabs 150 are set forth in Fig. 4a. As set forth in Figs. 4b and 4c, the floating gate slabs 150 preserve the tunnel dielectric 138 and provide the required coupling for cell programming to word lines. In the preferred embodiment, an anisotropic reactive ion etch step is used to etch through the poly 1. The poly 1 etch mask is subsequently stripped.

The process 200 continues with the creation of an interpoly dielectric 140 (step 214). The interpoly dielectric 140 covers the exposed areas of the floating gate slabs 150. As previously described, in the preferred embodiment, the interpoly dielectric layer is a composite layer of ONO. This layer is produced by a first oxidation step which oxidizes the exposed floating gate slabs 150 surfaces following the poly 1 etch (step 212). A layer of silicon nitride is then deposited. The silicon nitride is subsequently oxidized to produce another layer of silicon dioxide. In the preferred embodiment, the bottom oxide layer has a thickness in the range of 50-150Å, and is formed by a dry oxidation at  $\sim 1000^{\circ}\text{C}$ . The middle nitride layer is formed by conventional silicon nitride deposition techniques. In the preferred embodiment the initial thickness of the nitride layer is in the range of 75-150 Å. Oxidation of the of the nitride is a wet oxidation at a temperature of approximately  $950^{\circ}\text{C}$ . The resulting top oxide layer has a thickness in the range of 20-50Å. A high pressure oxidation can also be used to obtain a thicker top oxide layer greater than 50Å. Referring once again to Fig. 10, following step 214, the entire flash EPROM cell array is covered by an array protect mask (step 216). With the array

protected from etch steps, initial gate areas for peripheral transistor structures are formed by etching channel regions, and growing gate oxide for MOS transistor devices peripheral to the flash EPROM cell array. Once the intergate dielectric is formed, the second layer of polysilicon (poly 2) **134** is deposited (step **218**). The poly 2 layer **134** conformally covers the interpoly dielectric **140**, and so follows the general shape of the floating gate slab **150**. In the preferred embodiment, the poly 2 layer has a thickness of approximately 1k-2kÅ. The layer has a polycrystalline grain structure and is deposited at a temperature of approximately ~630°C. Doping is achieved either by in situ doping, or by ion implantation in the same manner as the poly 1 layer. In the preferred embodiment, following the deposition of the poly 2 layer, the layer of silicide **136** is formed. According to well understood techniques, a layer of tungsten silicide is formed over the poly 2 layer to create a WSi<sub>2</sub>/poly 2 layer. In the preferred embodiment, the silicide is deposited by chemical vapor deposition for a thickness of approximately 1000-1500 Å. The flash EPROM array following this step is set forth in Figs. 5a-5c. To prevent the silicide from lifting off in subsequent process steps, a layer of oxide, having a thickness of approximately 500 Å formed from tetraethylorthosilicate (TEOS), is deposited over the stacked gate. An insulating cap layer **146** is then formed over the silicide **136**/poly 2 **134** layer. The insulating cap layer **146** can be formed from TEOS for a total thickness of 1,000 Å. Alternatively, the insulating cap layer **146** can be a 500 Å layer of CVD nitride.

Referring once again to Fig. 10, the process continues with a stacked gate etch step (step **220**). A stacked gate etch mask of photoresist is formed over the insulating cap layer. The stacked gate etch mask defines the word lines of the array, and runs in strips, also defining the memory cell channel lengths. Once the stacked gate etch mask is formed, an anisotropic stacked gate etch is applied. The stacked gate etch etches through the exposed portions of the silicide **136**/poly 2 **134** layer and the floating gate slabs **150**, down to the field oxide **120** (or tunnel dielectric **138** in the event the active area **124** is underneath). The etching of the floating gate slabs **150** by the stacked gate etch creates the floating gates **110**. The etching of the silicide **128**/poly 2 **126** layer results in the overlying wordlines **112** (control gates). Following the array stacked gate etch, periphery gates are etched using a periphery gate mask and etch. Following the stacked gate etch (step **220**) and periphery gate etch, thin protective sidewall spacers are formed on the stacked gate by depositing a layer of oxide using TEOS, and subsequently etching the oxide layer back with an anisotropic etch. The stacked gate structures are then oxidized

to surround the floating gates with a good quality thermal oxide. It is noted that the floating gate is oxidized through the TEOS sidewalls.

The array is then subjected to a source implant (step 222) followed by a drain implant (step 224). In the preferred embodiment, a source implant mask is formed over the array that leaves the source regions exposed. Two source implants are then performed. Arsenic (As) is implanted at an approximate concentration and energy of  $8 \times 10^{15}/\text{cm}^2$  and 50KeV, respectively, and phosphorous is implanted at an approximate concentration and energy of  $1 \times 10^{14}/\text{cm}^2$  and 100KeV, respectively. Tilt source implant may be used as set forth in U.S. Patent No. 5,518,942 issued to Ritu Shrivastava one May 21, 1996. Following the source implant the source mask is removed and a drain mask is formed over the array which leaves the drain regions exposed. The drain is then implanted with two implants. One implant is of As at an approximate concentration and energy of  $3 \times 10^{15}/\text{cm}^2$  and 60KeV, respectively. Another implant is of boron at an approximate concentration and energy of  $4 \times 10^{13}/\text{cm}^2$  and 80KeV, respectively. Tilt implant may be used again in the formation of the drain. The flash EPROM device is then subjected to an anneal step, according to well understood techniques, to anneal any implant damage and allow for some diffusion of the dopants.

A sidewall dielectric is then deposited (step 226) and etched back (step 228) using conventional techniques to form source sidewall spacers 144 and drain sidewall spacers 142. The flash EPROM array following these steps is set forth in Figs. 6a-6c. As set forth in Fig. 6a, the source and drain implants (steps 222 and 224) result in the formation of the drain regions (114b,l-114d,n) and source regions (118a-118f), which in turn, completes the formation of the memory cell (108a,l-108d,n) structures.

Referring now to Fig. 10 in conjunction with Figs. 7a-7c, the process continues with a first interlayer dielectric (ILD 1) deposition (step 230). The ILD 1 148 conformally covers the memory cells (108a,l-108d,n), including the drain regions (114b,l-114d,n) and source regions (118a-118f). In the preferred embodiment the ILD 1 is silicon oxide deposited using conventional techniques with TEOS. The thickness of the ILD 1 is approximately 2,000 Å.

The preferred embodiment of the present invention diverges from prior art approaches in the etching of the self-aligned source contact. As shown in Fig. 10, a self-aligned source contact etch (step 232) is applied to the array to clear the source regions (118a-118f). A source etch mask 152 is formed over the flash EPROM array that exposes the source regions. In the preferred embodiment, the



source etch mask **152** exposes the source regions (**118a-118f**) along with portions of the isolation regions **120** between adjacent source regions. Further, because the source contact is self-aligned, the source etch mask **152** also exposes the source sidewall spacers **144** and a portion of the cap insulators **146**. Also note that this opening can overlay the stacked gate without introducing any problems. A source etch is then applied. Unlike the self-aligned common source approach of Figs. 1b and 1c, the source etch does not etch through the portions of the field oxide regions **120** that separate adjacent source regions. Instead, the source etch clears the ILD **1** **148** over the source regions to expose the source regions, leaving the intermediate field oxide regions **120** in-tact. This results in minimal etching of the isolation regions **120**, but more importantly, results in far less reduction of the thickness of the source sidewall spacers **144** than the noted prior art self-aligned common source case of Figs. 1b and 1c. The flash EPROM array following the source contact etch is set forth in Figs. 8a-8c. In an alternate embodiment, the source etch mask exposes only those areas proximate the source regions, rather than an entire horizontal swath. The extents of the this alternate source etch mask are represented by the dashed line in Fig. 8a.

Once the source regions (**118a-118f**) have been cleared by the source contact etch (step **232**), a third layer of polysilicon (poly 3) **126** is deposited (step **234**) to form self-aligned contacts with the source regions (**118a-118f**). A layer of silicide **128** is then formed over the poly 3 **126** (step **236**). The poly 3 **126**/silicide **128** layer is then patterned (step **238**) to clear areas between the rows to allow for bit line contacts, while maintaining a conductive connection between multiple source regions (**118a-118f**). In the preferred embodiment, the poly 3 **126**/silicide **128** layer is patterned into source conductor members **122a-122b** which are disposed in the row directions, over the source regions shared by adjacent rows. It is noted that the silicide **128** reduces the resistance between the commonly connected sources. Further, the diffused source region area is much smaller than that of the prior art approaches in Figs. 1a-1c, resulting in less substrate leakage. Also, due to the silicided poly 3, the source resistance can be made much smaller than the case of conventional source diffusions. The EPROM array following the poly 3 **126**/silicide **128** etch is set forth in Figs. 9a-9c. As set forth in Fig. 9b, in the row direction along the source regions, the poly 3 **126**/silicide **128** layer is disposed over the isolation regions **120** and extends to make contact with the source regions. As set forth in Fig. 9a, the source conductor member **122a** extends between the wordline **112**/floating gate **110** pairs, to make contact with the source region **118b**.

The source sidewall spacers 144 and insulator caps 146 insulate the wordlines 112 and floating gates 110 from the source conductor member 122a, in a self-aligned contact arrangement. The relatively wide source conductor members 122a-122b allow for more flexibility in the event a via is dropped to the source conductor members 122a-122b from a higher level of interconnect such as metal. Further, such a via would consume no substrate area, unlike the self-aligned common source arrangement set forth in Figs. 1b and 1c. In the preferred embodiment, the poly 3 is deposited and doped using conventional chemical vapor deposition techniques for a thickness of approximately 1,000 Å. The silicide is tungsten silicide, and is deposited by chemical vapor deposition for a thickness of approximately 1,000 Å.

Once the source conductor members 122a-122b have been formed, a second interlayer dielectric (ILD 2) 130 is deposited over the flash EPROM array. In the preferred embodiment the ILD 2 is formed using boron and phosphorous doped TEOS (BPTEOS), or alternately, conventional borophosphosilicate glass (BPSG) is used. The thickness of this ILD is approximately 4,000 Å after reflow and/or planarization using chemical mechanical polishing (CMP) techniques. Bit line contacts (116a-116f) are then formed (step 242) by etching through the ILD 1 148 and ILD 2 130 to the active areas between the drain regions of the rows. A first layer of metallization (metal 1) is then deposited to make contact with the bit line contacts (116a-116f) (step 244). The metal 1 is then patterned according to conventional techniques (step 246) to form bit lines 132 as set forth in Figs. 2a-2c. In the preferred embodiment, a tungsten "plug" is formed, using tungsten deposition and etch back techniques, to make bit line contacts with the drain regions. The process concludes with conventional EPROM processing techniques (step 248) to arrive at a flash EPROM device. Such techniques can include more layers of metal interconnects, if needed.

Unlike prior art flash EPROM architectures, the present invention provides an EPROM array having very low resistance source lines running in the row direction. For example, the sheet resistance of the source interconnect can be reduced from about 80Ω/ to 8Ω/ using the present invention. As a result the number of metal "straps" required to provide a reference voltage to the source lines can be eliminated or reduced, freeing up area in the array.

The architecture of the present invention also allows the array to be broken into customizable groups of one or more rows by source decoding. In this manner, a user may selectively erase various sectors of arbitrary sizes (i.e., programmable erase granularity). For example, in prior art approaches, to erase selected rows in

a given common source region (or "sector") the entire common source region (i.e., all the sources in the sector) would be driven to a source erase voltage (a positive voltage, for example) while selected wordlines (those rows that are to be erased) were driven to a wordline erase voltage (a relatively large negative voltage, for example). Those rows within the sector that were not be erased would have wordlines driven to wordline de-select voltage, but would still have their sources driven to the source erase voltage. In contrast, by using decoded sources, the present architecture allows the wordlines and sources of only those rows that are to be erased, to be driven to the wordline erase voltage and source erase voltage, respectively. The number of rows that may be erased in this manner is not limited to a certain minimum number due to a common source diffusion, but can be determined by a user of the flash EPROM device. Such an architecture provides the selectable erase advantages of conventional EEPROMs with the rapid erase advantages of conventional flash EPROMs. Providing this new flexibility can also improve reliability by better control of erase, and erase convergence techniques.

Fig. 11 sets forth a block schematic diagram illustrating a source decoding scheme for a flash EPROM according to the present invention. The flash EPROM is designated by the general reference character **300**, and includes an array of 1-T memory cells **302** arranged in rows and columns. The memory cell in the array **302** are commonly coupled by their respective drains to bit lines **304** along the column direction (the vertical direction in Fig. 11). The control gates of the memory cells of the array **302** are commonly coupled word lines **306** in the row direction (the horizontal direction in Fig. 11). The sources of the memory cells of the array **302** are commonly coupled source lines **308** which, in the embodiment of Fig. 11, are disposed in the row direction. It is further noted that the source lines **308** in Fig. 11 are shared by two adjacent rows of memory cells.

Referring once again to Fig. 11, the source lines **308** are each coupled to, and driven by, a source driver section **312**. The source driver section **312** includes a source driver circuit **312** coupled to each source line **308**. It is understood that alternate embodiments could include source drivers coupled to multiple source lines. Each source driver circuit **312** receives an input signal from a source decoding section **314**, and in response to the input signal, drives its respective source line **308** to a source programming voltage ( $V_{sp}$ ), a source erase voltage ( $V_{se}$ ) or a source read voltage ( $V_{sr}$ ) depending upon the current operating mode of the flash EPROM **300**.

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The source decoding section **314** is shown to receive a number of address predecode signals **316**. According to well understood techniques, address predecode signals **316** are generated from externally applied address signals. In the preferred embodiment, the address predecode signals **316** are the same as those used to drive word line drivers (i.e., are row predecode signals). The address predecode signals **316** are received by a programmable decode value circuit **318**, which also receives user input values **320**. The programmable decode value circuit **318** provides a number of source decode signals **322** based upon the address predecode signals **316** and the user input values **320**. In the particular embodiment of Fig. 11, the source decode signals **322** generally follow the address predecode signals **316** unless altered in response to the user input values **320**, which can force certain source decode signals **322** to a predetermined logic state, regardless of values of the address predecode signals **316**. For example, if the user input values indicate no alteration source decode signals, the programmable decode value circuit **318** is essentially transparent in operation, allowing the predecode signals **316** to drive a given source decoder **324**. In such a case the memory cell of the array **302** could be erased in groups of two rows only. Alternately, the user input values **320** could dictate a larger logical grouping of source line **308**, to allow for the simultaneous erasure of multiple row pairs. Finally, the user input values **320** could indicate entire sector or array erase, in which case the address decode values would have no effect on the source decode signals **322**, and the source decoder signals **324** would all be driven at the same time for a standard sector/array flash erase operation.

It is understood that while Fig. 11 sets forth only four address predecode signals **316** one skilled in the art could arrive at equivalent structures utilizing fewer or greater numbers of address predecode signals. Further, one source decoder **324** could drive multiple source drivers **312**. It is also noted that the source decode signals **312** could be generated entirely from the user input values **320**, allowing the source lines **308** of memory cell array **302** to be logically divided by groups of rows, into arbitrary fractional ( $1/2^n$ ) portions of the array, where the value  $n$  is provided by user input values **320**.

The user input values **320** could be provided the flash EPROM **300** by way circuits altered via laser fusible links. Non-volatile memory cells could also be employed to store the user values.

By greatly reducing the role of substrate resistance in the common source arrangement, source voltage drops are reduced improving the uniformity of



## IN THE CLAIMS

What is claimed is:

- 5     **1.**     A non-volatile memory array, comprising:
- a plurality of memory cells arranged in at least one row and at least one column, each memory cell including a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate disposed over the floating gate, the floating gate; and
- 10           at least one conductive member disposed along at least a portion of the row, said conductive member making contact with the sources of the memory cells of the portion of the row, said conductive member being self-aligned with the memory cells of said portion of the row.
- 15     **2.**     The non-volatile memory array of claim **1**, wherein:
- said plurality of memory cells includes a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source with at least one memory cell of the second row; and
- 20           said conductive member is disposed along at least a portion of the first and second rows and makes contact with the common sources of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows.
- 25     **3.**     The non-volatile memory array of claim **1**, wherein:
- said plurality of memory cells includes a plurality of row pairs, at least a portion of the memory cells in each row pair having common source regions; and
- 30           a conductive member associated with each row pair, each conductive member being disposed along said portion of its respective row pair and making contact with the common sources thereof, the contact of each conductive member being self-aligned with the of the memory cells of said portion of its respective row pair.
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4. The non-volatile memory array of claim 1, wherein:

said memory cells are arranged in a plurality of rows, the control gates of the memory cell in each row being commonly coupled to a word line extending generally parallel to the row; and

5 a conductive member associated with at least one row, each conductive member being disposed generally parallel to the word line along at least portion of its respective row and making contact with the source regions thereof, the contact of each conductive member being self-aligned with the memory cells of said portion of its respective row.

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5. The non-volatile memory array of claim 4, wherein:

each said conductive member overlaps the word line of its associated row along at least said portion of its respective row.

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6. The non-volatile memory array of claim 4, wherein:

the plurality of rows includes pairs of adjacent rows, at least a portion of the memory cells of the pairs of adjacent rows sharing common source regions; and

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each said conductive member is associated with a pair of adjacent rows, and is disposed generally parallel to the word lines of its respective pair of adjacent rows along at least a portion of pair of adjacent rows and makes contact with the common source regions thereof, each said conductive member overlapping the word lines of its associated pair of adjacent rows along at least said portion of its respective pair of adjacent rows.

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7. The non-volatile memory array of claim 1, wherein:

said conductive member includes polysilicon.

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8. The non-volatile memory array of claim 7, wherein:

said conductive member includes a metal silicide.

9. The non-volatile memory array of claim 7, wherein:

said conductive member includes a metal.

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10. The non-volatile memory array of claim 1, including:

a plurality of conductive members; and  
a source decoder and driving circuit for driving selected conductive members to an erase voltage in response to a plurality of source decode signals.

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**11.** The non-volatile memory array of claim 10, including:  
the plurality of source decode signals are generated in response to at least one memory address signal.

10 **12.** The non-volatile memory array of claim 10, including:  
the plurality of source decode signals are generated in response to at least one user determined value.

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13. In a flash erasable EPROM, a compact array, comprising:
- a substrate;
  - a first flash erasable electrically programmable read-only memory (EPROM) cell formed on the substrate, and including a first cell top, a first cell first side, and a second cell second side opposite to the first cell first side;
  - a first cap insulator formed over the first cell top of said first flash EPROM cell;
  - a first insulating sidewall formed on the first side of the first flash EPROM cell; and
  - a conductive member disposed on at least a portion of said first insulating sidewall and making contact with a contact portion of the substrate adjacent to the first insulating sidewall.
14. The compact array of claim 13, wherein:
- said first flash EPROM cell includes a first floating gate, a first interlayer dielectric and a first control gate formed over the first floating gate on the first interlayer dielectric.
15. The compact array of claim 13, wherein:
- said conductive member includes a first layer of doped polysilicon.
16. The compact array of claim 13, wherein:
- said conductive member includes a layer of metal silicide.
17. The compact array of claim 13, including:
- a second flash EPROM cell formed adjacent to the first flash EPROM cell, the second flash EPROM cell including a second cell top, a second cell first side and second cell second side, the second cell second side opposing the first cell first side across the contact portion of the substrate;
  - a second cap insulator formed over the second cell top of said second flash EPROM cell;
  - a second insulating sidewall formed on the second side of the second flash EPROM cell; and



20. In a flash EPROM memory device formed on a semiconductor substrate, an array configuration, comprising:

a plurality of flash EPROM cells arranged in an array having a plurality of rows extending in a row direction;

a plurality of source contacts formed along at least one row of the array, each said source contact being separated from an adjacent source contact by a substrate isolation region; and

a source connecting member extending in the row direction, disposed over, and making contact with, said plurality of source contacts.

21. The array configuration of claim 20, wherein:

said plurality of source contacts are formed along row pairs, each said source contact being shared by one flash EPROM cell of one row of the row pair and one flash EPROM cell of the other row of the row pair

22. The array configuration of claim 20, including:

a plurality of bit line contacts formed along at least one row of the array, opposite to said source contacts.

23. The array configuration of claim 20, including:

said source contacts are double diffused.

24. The array configuration of claim 20, including:

each flash EPROM cell includes a floating gate, the array further including a word line disposed along at least one of the rows, over and insulated from the floating gates of the row; and

and said plurality of contacts are self-aligned with the said word lines and the floating gates of the row.

25. The array configuration of claim 20, including:

a plurality of source connecting members; and

means for coupling a predetermined group of source connecting members to an erase voltage in response to a plurality of source decode signals.

26. The array configuration of claim 25, wherein:

said means for coupling includes

5 a plurality of source driver means for coupling at least one source connecting member to the erase voltage in response to driver input signal, and

a source decoder means for generating at least one driver input signal in response to the source decode signals.

27. The array configuration of claim 26, including:

10 address dependent source decode signal generating means responsive to a plurality of memory address signals for generating the source decode signals.

28. The array configuration of claim 26, including:

15 user dependent source decode signal generating means responsive to a plurality of predefined user values for generating the source decode signals.

29. The array configuration of claim 26, including:

20 configurable source decode signal generating means responsive to a plurality of predefined user values and memory address values for generating the source decode signals.

## ABSTRACT

A flash EPROM array (100) and method of manufacture is disclosed. Source regions (118a-118f) are shared between the memory cells (108a,l-108d,n) of row (104a-104d) pairs, and are isolated from one another in the row direction by isolation regions 120. Low resistance source conductor members (122a-122b) extend in the row direction and are formed over the source regions (118a-118f) and make contact therewith in a self-aligned fashion. The architecture allows for source decoding and thus enables user programmable sector erase architecture.

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**Declaration for Patent Application**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**FLASH EPROM ARRAY WITH SELF-ALIGNED SOURCE CONTACTS AND  
PROGRAMMABLE SECTOR ERASE ARCHITECTURE**

the specification of which

☒ is attached hereto.

☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_/\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(2) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

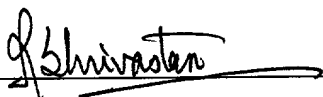
<u>Prior Foreign Application(s).</u>	
<u>Priority Claimed</u>	<u>Country</u> <u>Day/Month/Year Filed</u>
<input type="checkbox"/> Yes <input type="checkbox"/> No	
<input type="checkbox"/> Yes <input type="checkbox"/> No	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112. I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.58(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

<u>Application Serial Number</u>	<u>Filing Date</u>	<u>Status</u>
		<input type="checkbox"/> Patented <input type="checkbox"/> Pending <input type="checkbox"/> Abandoned
		<input type="checkbox"/> Patented <input type="checkbox"/> Pending <input type="checkbox"/> Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor **Ritu Shrivastava**

Inventor's signature 


Date 4/22/97

Residence: **44455 Parkmeadow Drive  
Fremont, California 94539**

Citizenship: **United States of America**

Post Office Address: same as residence

Full name of second inventor **Chitranjan N. Reddy**

Inventor's signature 

Date 4/22/97

Residence: **Los Altos Hills, California 94022**

Citizenship: **United States of America**

Post Office Address: **3099 North First Street  
San Jose, CA 95134**

Express Mail Label No. **EH 7138 32766 US**

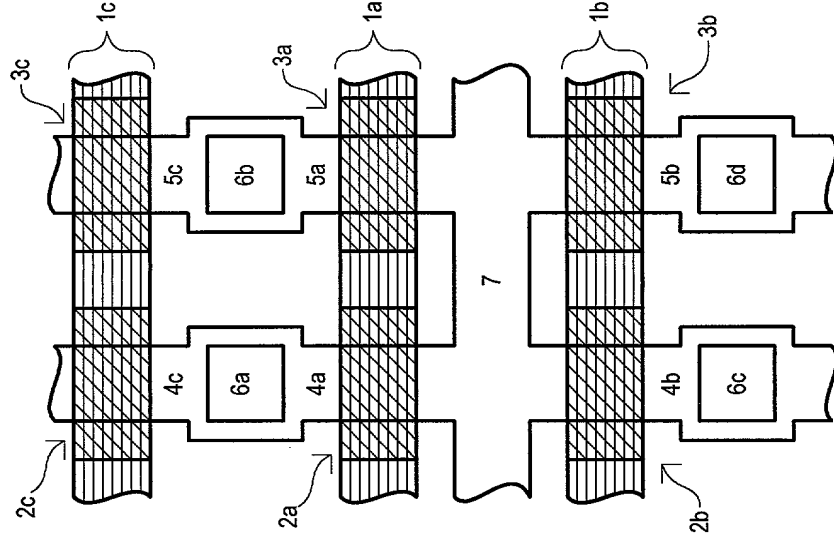


FIG. 1a

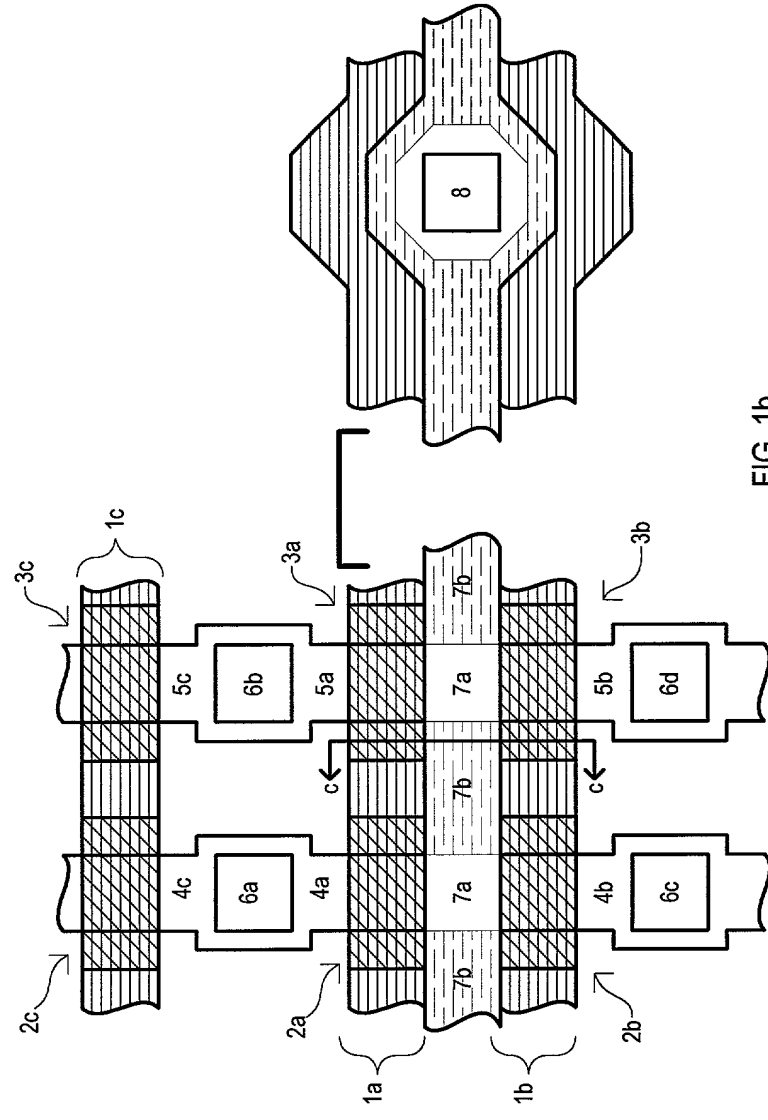


FIG. 1b

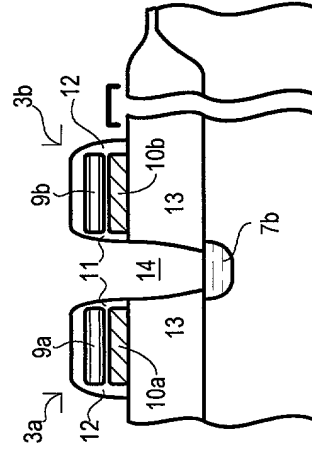


FIG. 1c



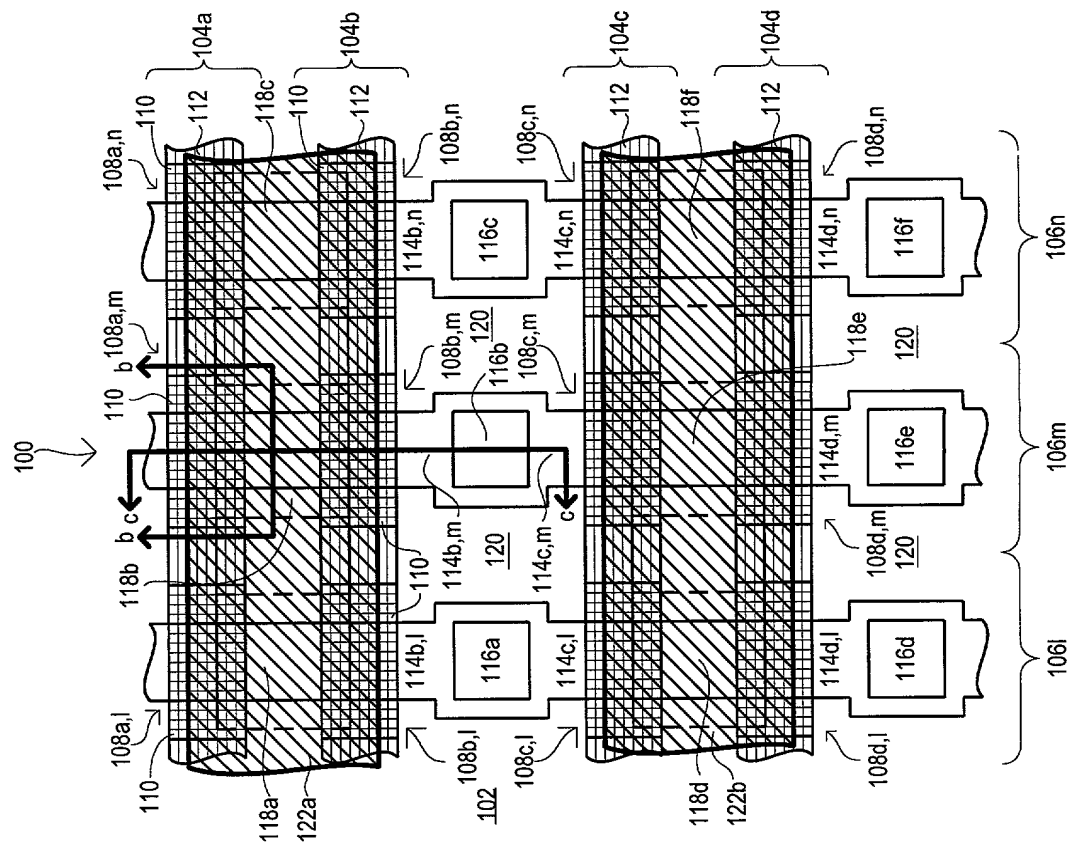


FIG. 2a

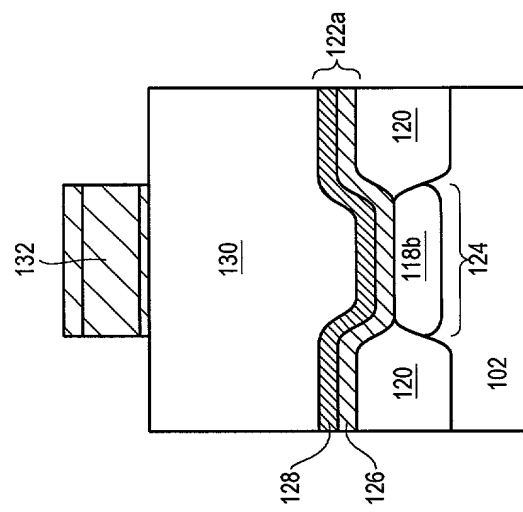


FIG. 2b

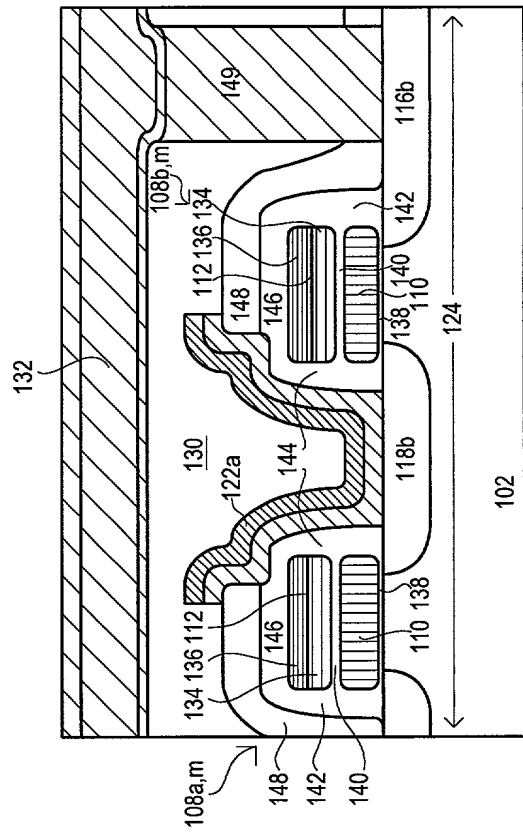


FIG. 2c

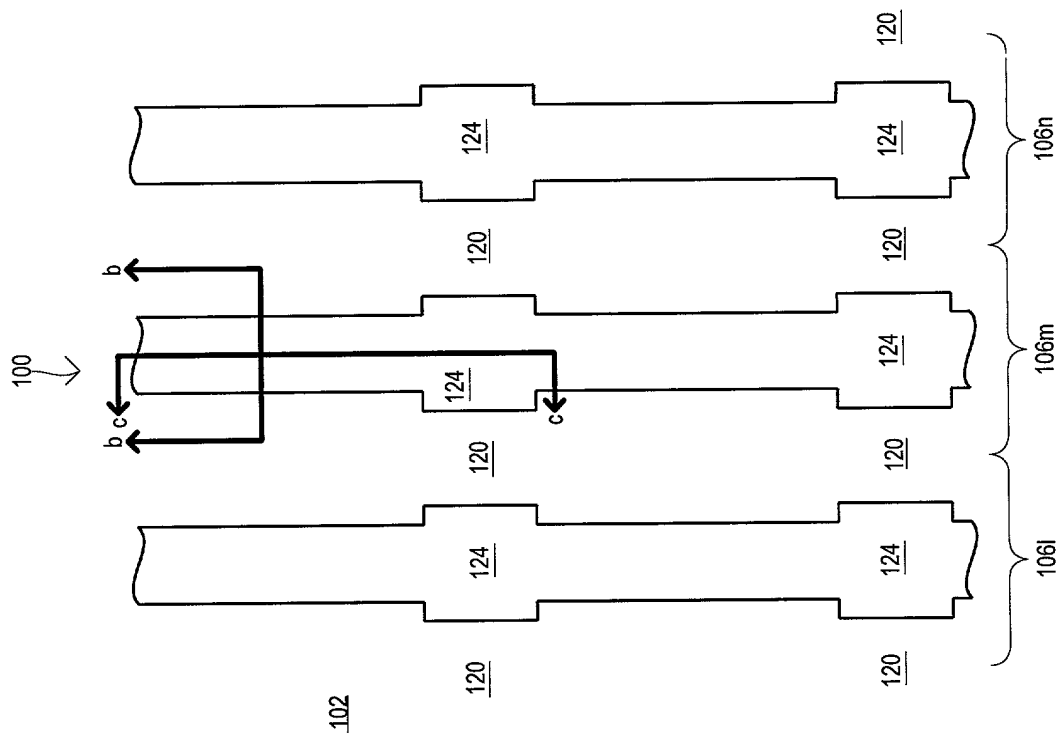


FIG. 3a

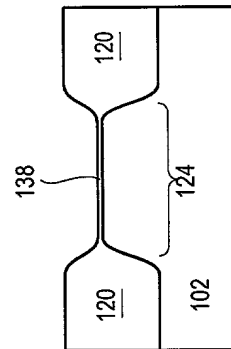


FIG. 3b

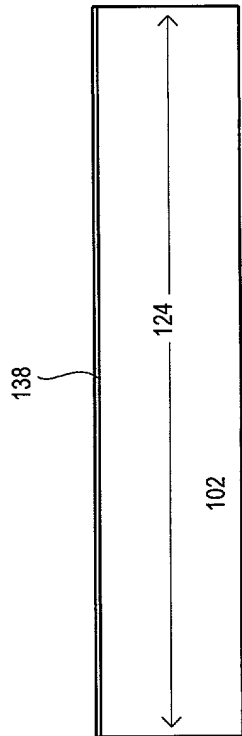


FIG. 3c

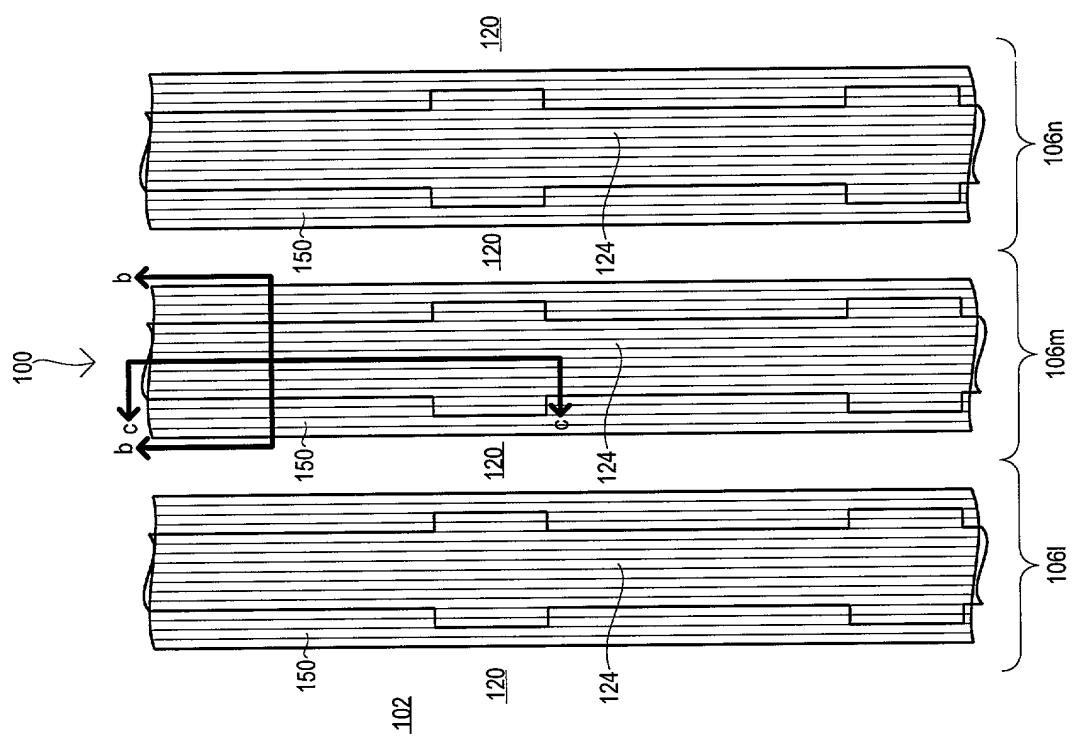


FIG. 4a

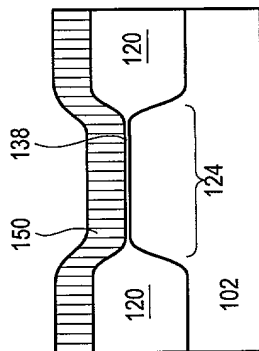


FIG. 4b

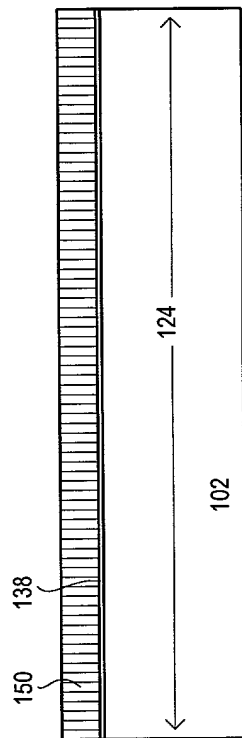


FIG. 4c



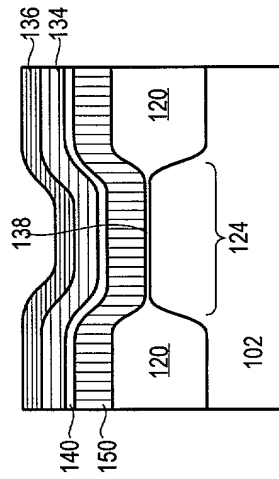


FIG. 5b

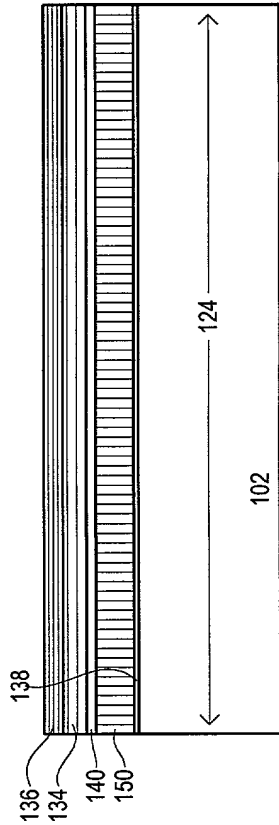


FIG. 5c



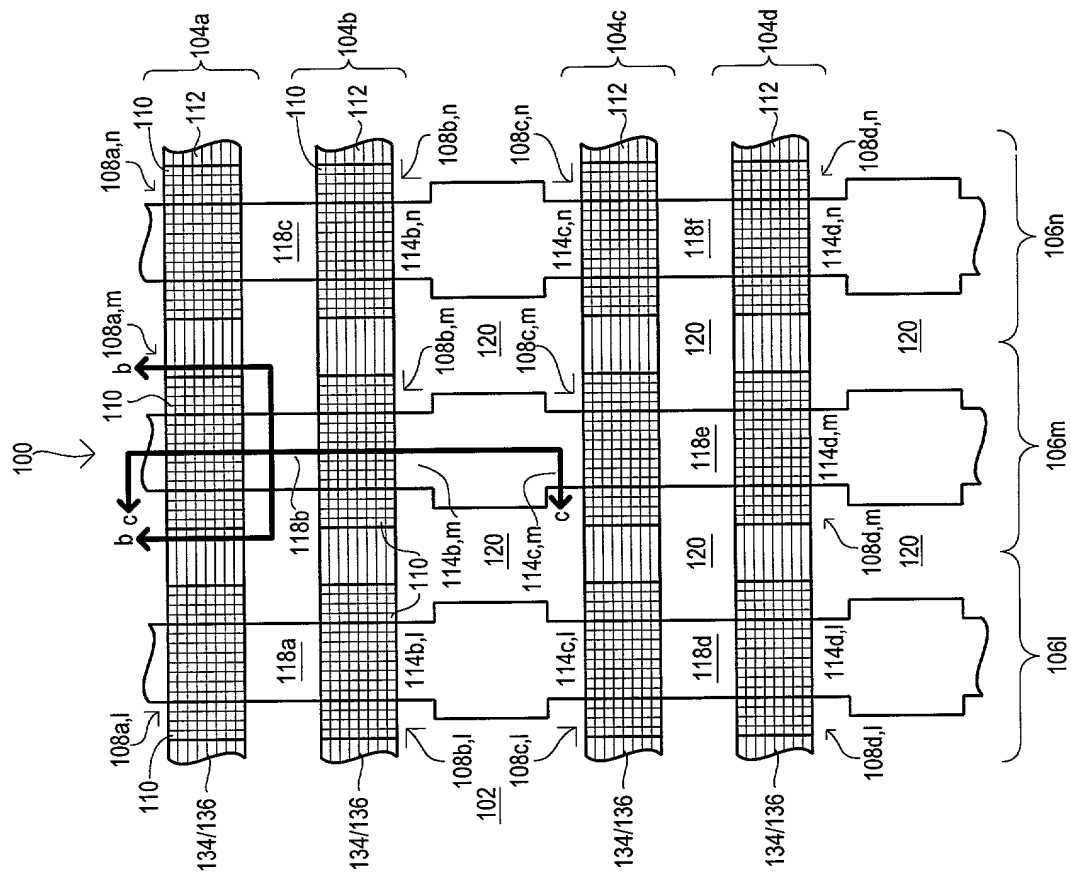


FIG. 6a

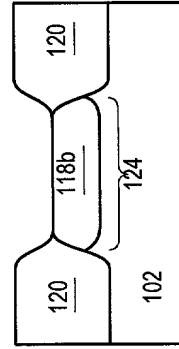


FIG. 6b

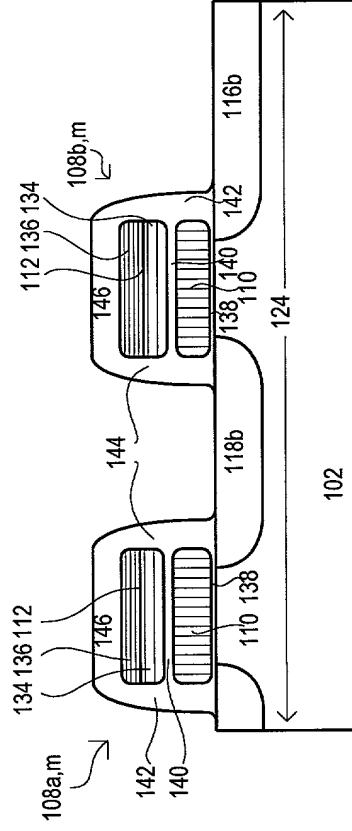


FIG. 6c

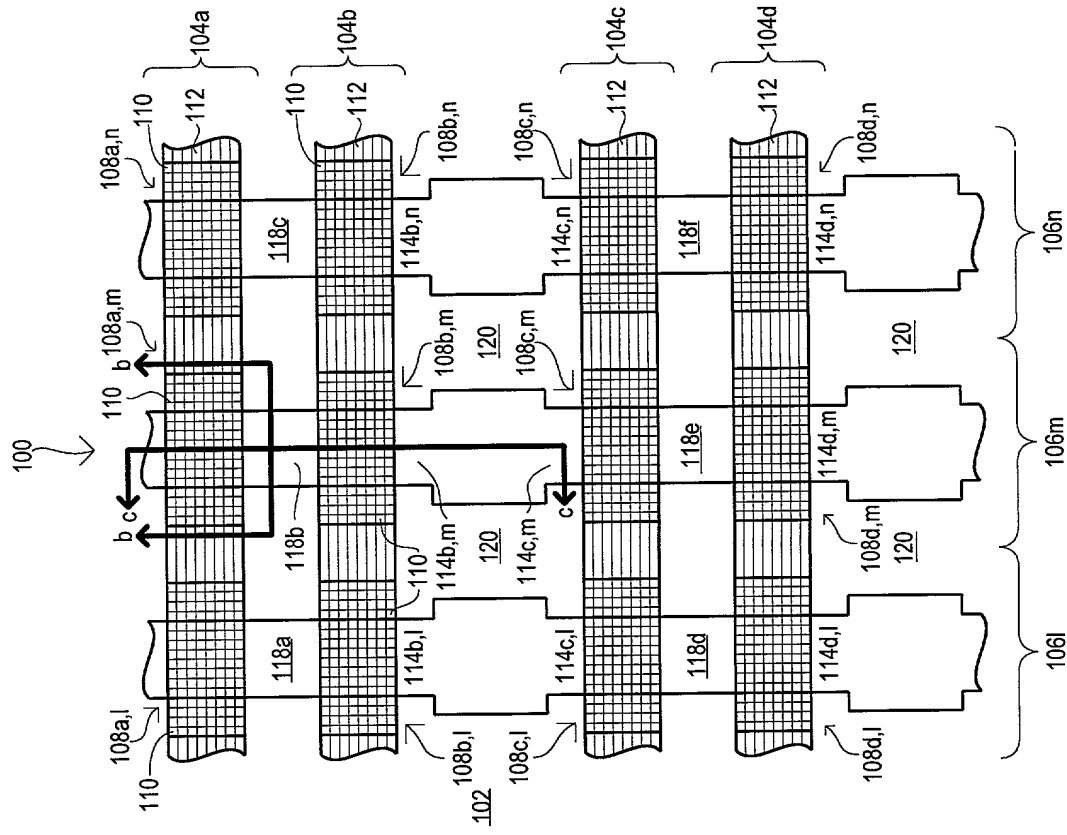


FIG. 7a

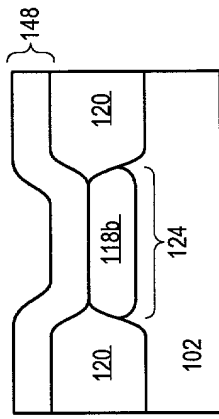


FIG. 7b

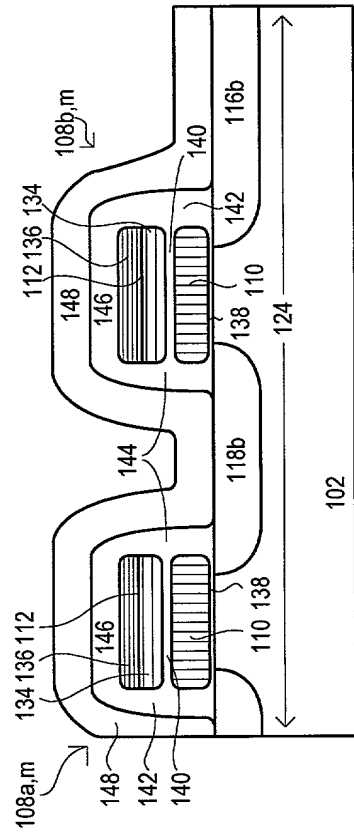


FIG. 7c

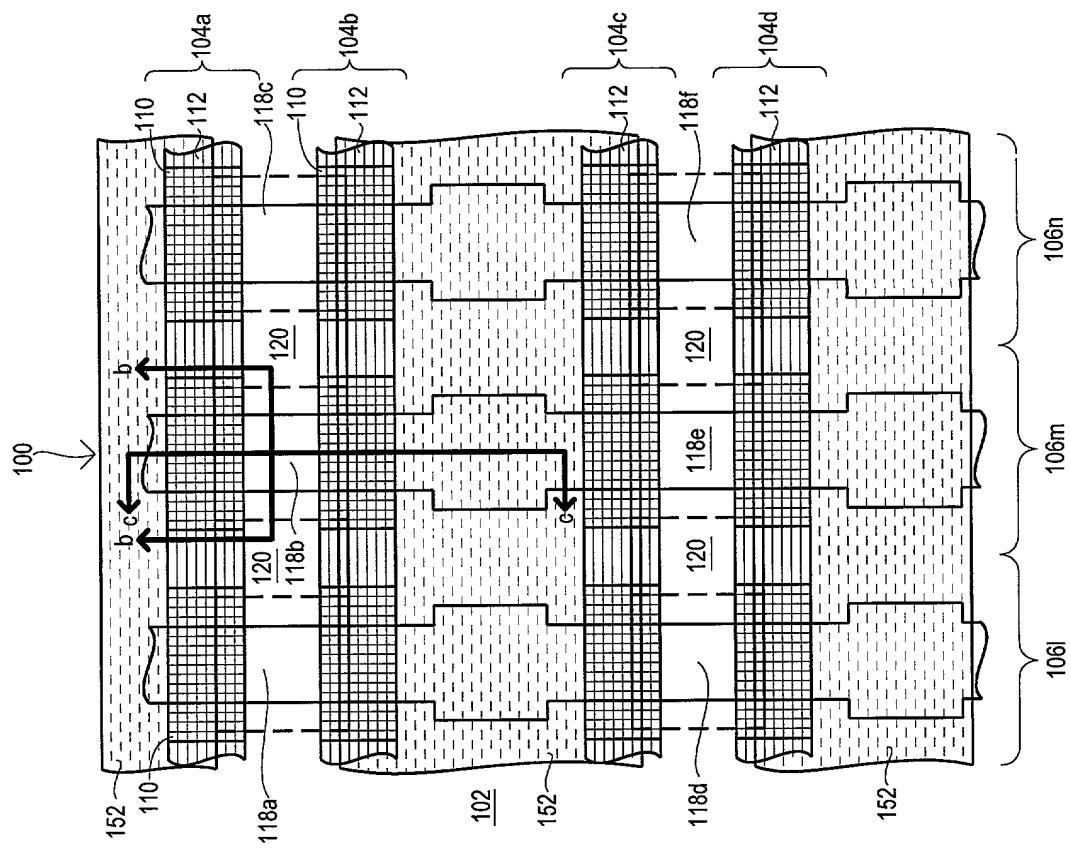


FIG. 8a

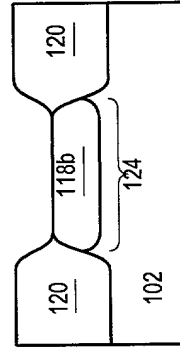


FIG. 8b

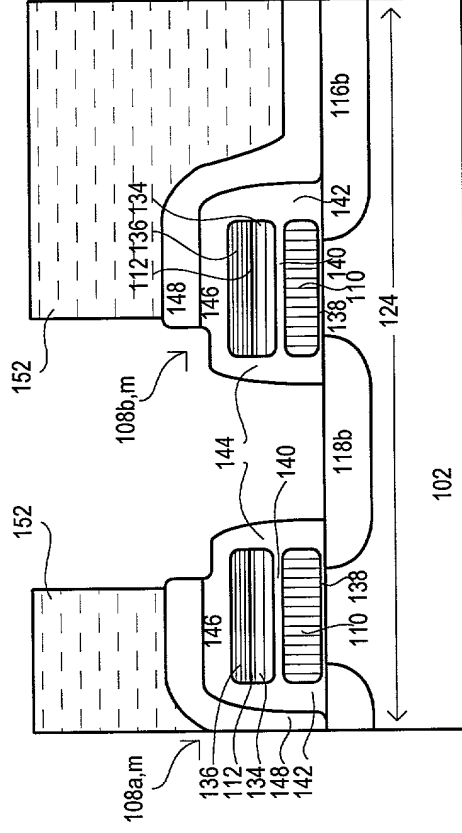


FIG. 8c

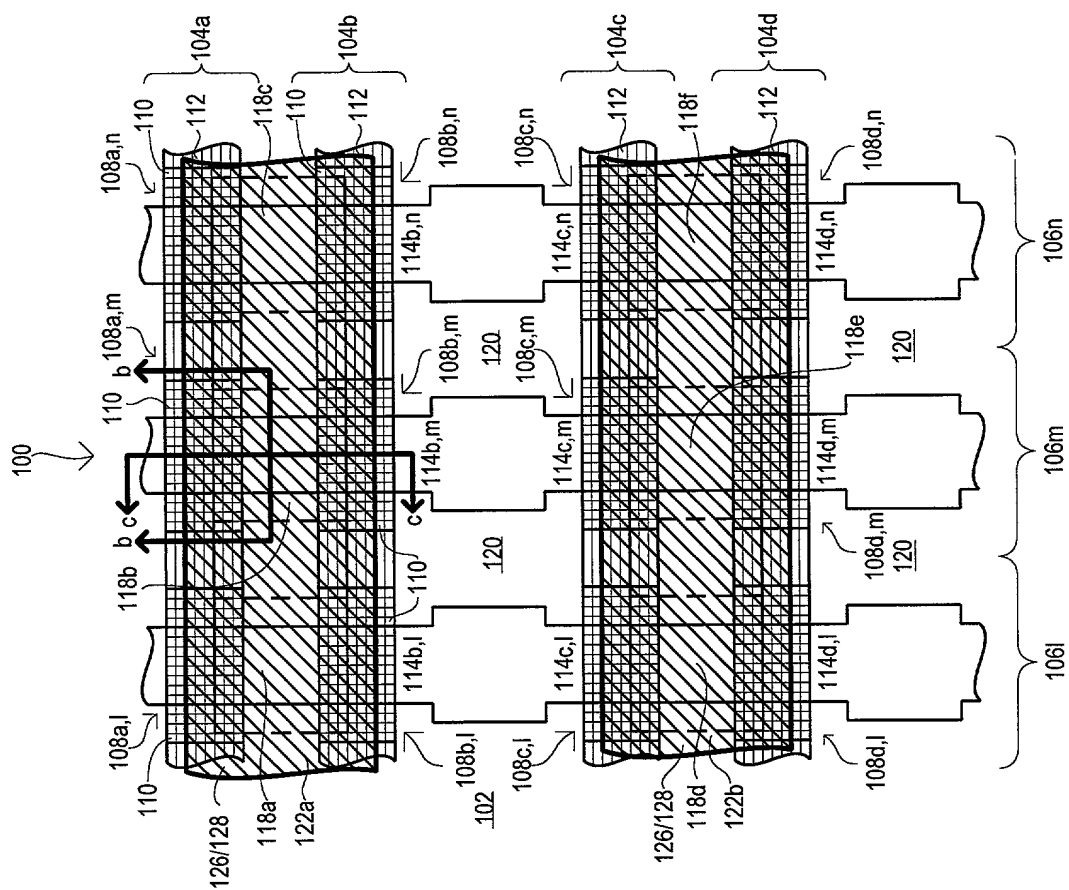
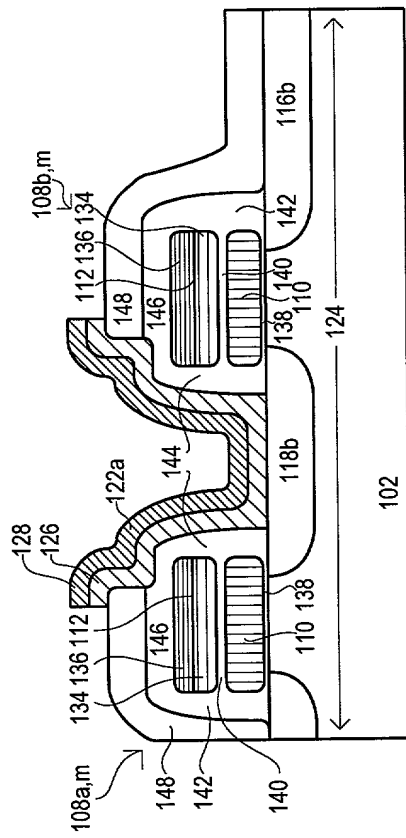
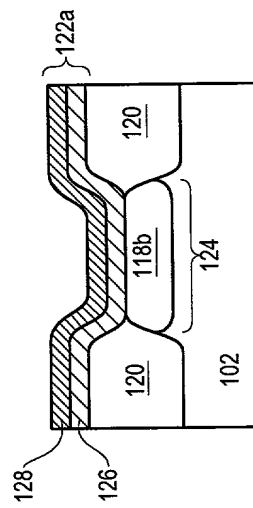
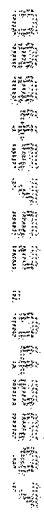


FIG. 9a





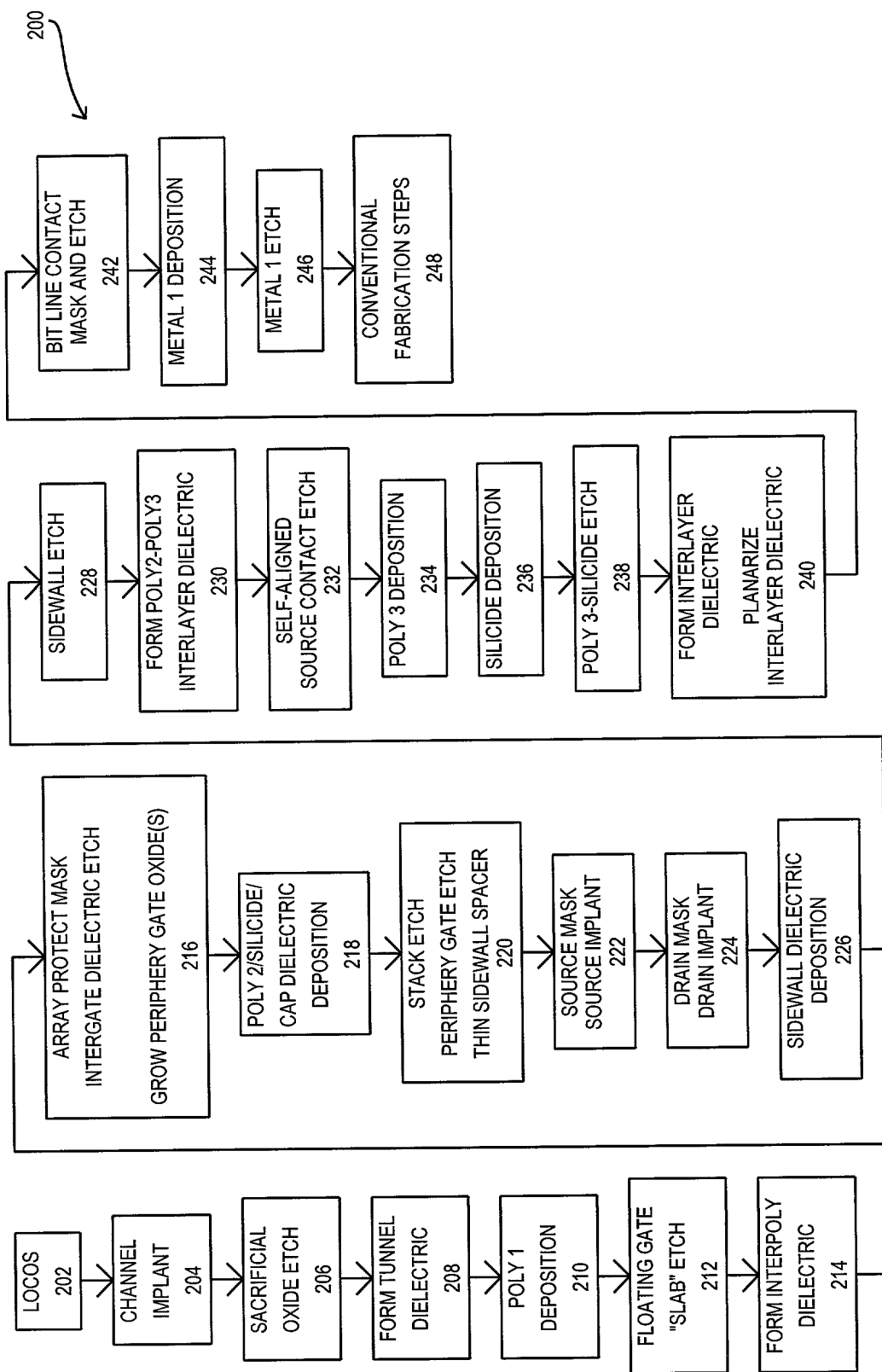


FIG. 10

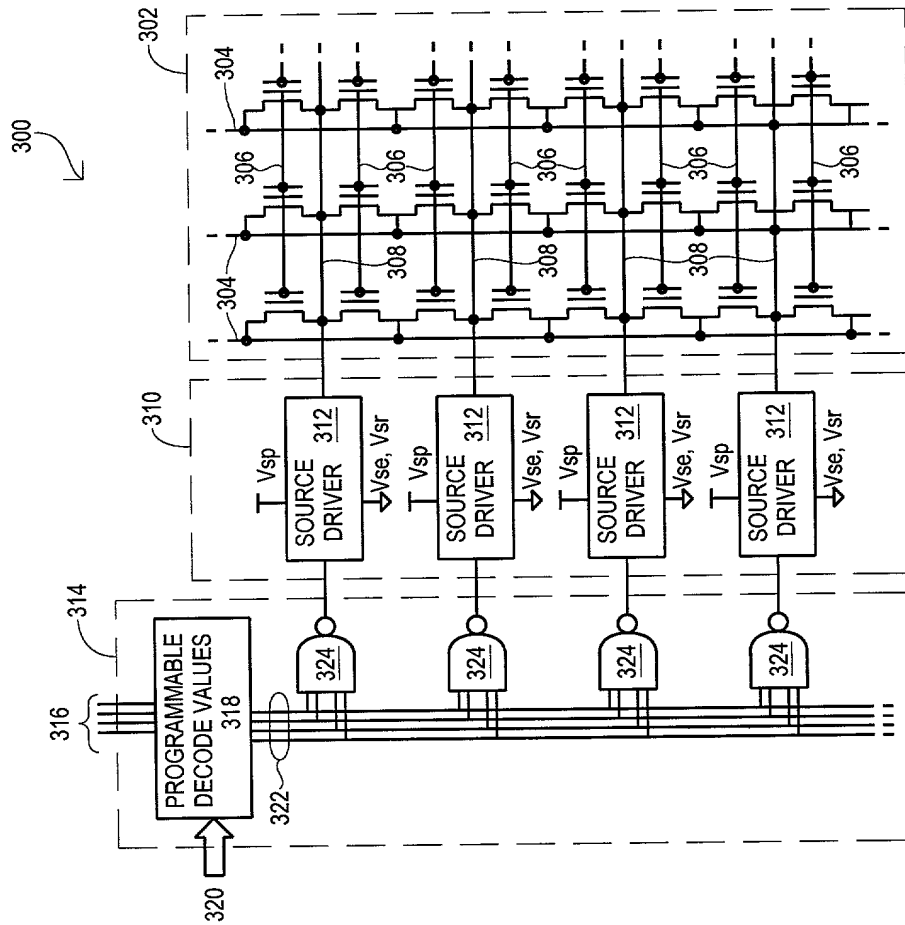


FIG. 11